

FIG. 1 is a schematic diagram of a prior art device 100. The device 100 includes a substrate 102, a first layer 104, a second layer 106, a third layer 108, a fourth layer 110, a fifth layer 112, a sixth layer 114, a seventh layer 116, an eighth layer 118, a ninth layer 120, a tenth layer 122, an eleventh layer 124, a twelfth layer 126, a thirteenth layer 128, a fourteenth layer 130, a fifteenth layer 132, a sixteenth layer 134, a seventeenth layer 136, an eighteenth layer 138, a nineteenth layer 140, a twentieth layer 142, a twenty-first layer 144, a twenty-second layer 146, a twenty-third layer 148, and a twenty-fourth layer 150.

Fig. 1
(Prior Art)

100

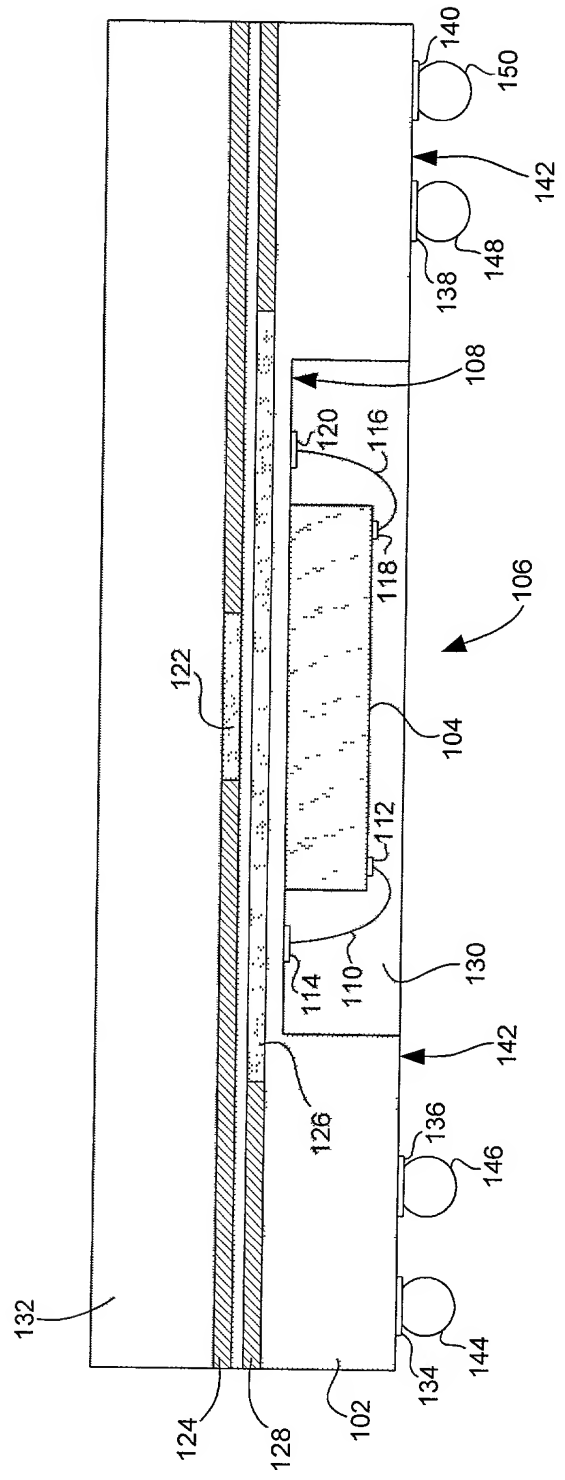


Fig. 2

FIG. 2 is a cross-sectional view of a semiconductor device 200, showing a substrate 202, a gate stack 204, and a channel layer 206. The device includes a source region 208, a drain region 210, and a gate electrode 212. The channel layer 206 is disposed between the source and drain regions. The gate stack 204 is disposed on top of the channel layer 206. The device is shown in a cross-sectional view along a line A-A.

200

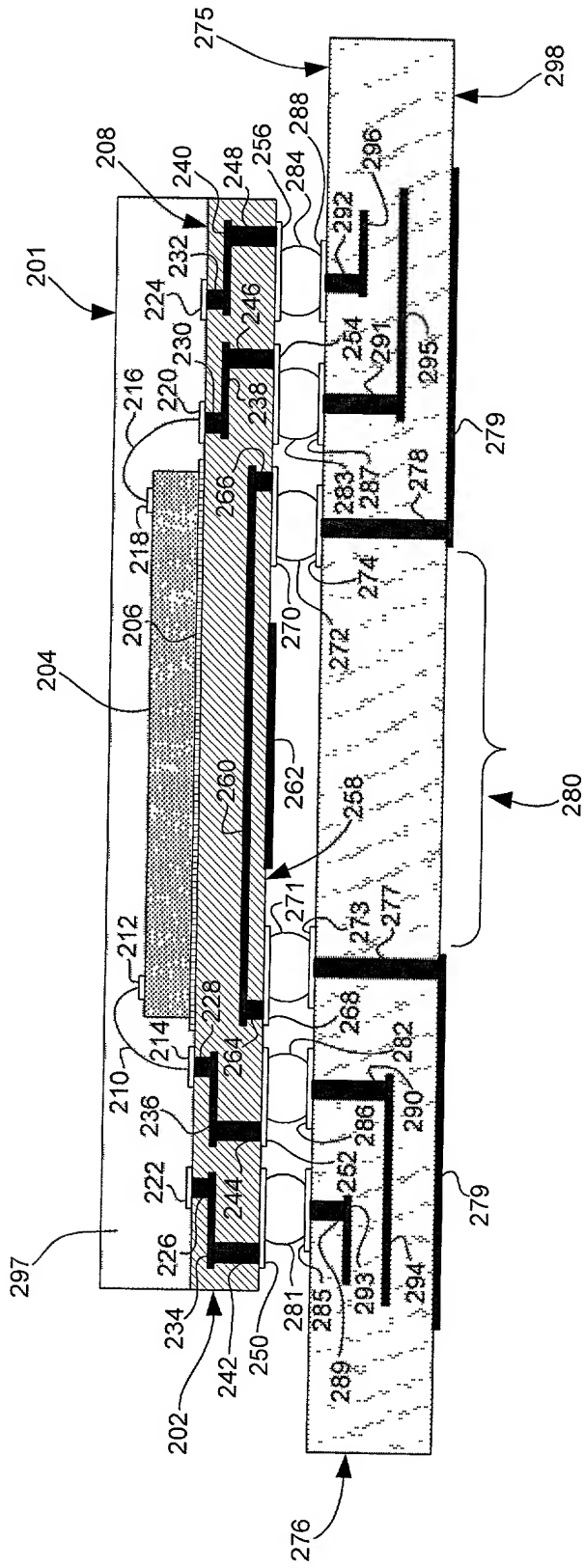


Fig. 3

